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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/438,247	11/12/1999	JUNJI NISHIGAKI	15162/01290	9067

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EXAMINER	
KASSA, YOSEF	
ART UNIT	**PAPER NUMBER**
2623	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/438,247	NISHIGAKI ET AL.	
	Examiner	Art Unit	
	YOSEF KASSA	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-14* is/are rejected.

7)☒ Claim(s) *4 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments see the remark on page 6-9, filed on September 23, 2005, with respect to rejections of claims 1-15 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made on Mita et al (U.S. Patent 5,692,210).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 5-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Mita et al (U.S. Patent 5,692,210).

With regard to claim 1, Mita et al discloses a plurality of processors (item 1603, in Fig. 30, comprises multiple processors, also refer to col. 17, lines 62-67) processing respective portions of the same input image data (note that block selected from the same input image data) in parallel with each other and outputting respective processed portions of said input image data (see col. 17, lines 62-col. 18, lines 1); and

an address memory storing address information related to a position of each

portion of said input image data within said input image data for each respective portion of image data being processed by said plurality of processors (see col. 18, lines 1-8).

With regard to claim 2, Mita et al discloses an image memory storing said image data output from said plurality of processors (refer to Fig. 30, items 1603 and 1602, the output from processors 1603 is stored in memory 1602, also see col. 17, lines 62-67), and read means reading (scanning) said image data from said image memory on the basis of said address information stored in said address memory (see col. 18, lines 65-col. 19, lines 5).

With regard to claim 3, Mita et al discloses further comprising an image memory storing said image data output from said plurality of processors along the sequence of addresses on the basis of said address information stored in said address memory (see col. 19, lines 1-18).

With regard to claim 5, Mita et al discloses wherein said plurality of processors also output arrangement information corresponding to said processed portions of said image data (see col. 19, lines 15-25).

Claim 6 is similarly analyzed and rejected the same as claim 1. Except, the additional limitation "a controller restoring a single image from plurality of data processed in plurality of processors in accordance with arrangement information" (see Fig. 39, the image data from writing-side image memory restoring the image data from the read-side memory).

With regard to claim 7, Mita et al discloses further including a second memory storing said data processed in said plurality of processors, wherein said controller reads

said data from said second memory in sequence along said arrangement information and restores said image (see col. 18, lines 34-45 also see Fig. 39).

With regard to claim 8, Mita et al discloses further including an image memory, wherein said controller stores processed data in positions of said image memory corresponding to said arrangement information (see col. 18, lines 34-45, refer to Fig. 30, the control circuit controlling arithmetic (processors) and the address generator for the arranging image data in output-side memory).

With regard to claim 9, Mita et al discloses first memory is provided in correspondence to each of said plurality of processors (see Fig. 30, item 1601 first memory connected to via 1604 to arithmetic block (processors) to process the divided image).

With regard to claim 10, Mita et al discloses wherein said plurality of processors also output arrangement information corresponding to processed said data when outputting said data (see col. 17, lines 64-col. 18, lines 3).

Claim 11 is similarly analyzed and rejected the same as claim 6.

With regard to claim 12, Mita et al discloses an input image data port and an input image address port for inputting (refer to Fig. 39, the output image data of control circuit is inputted to the processor unit), respectively, image data corresponding to a portion of an image and a position of the image data within the image (see col. 17, lines 56-67); and

an output image data port and an output image address port for outputting (refer to Fig. 30, which comprises output data section (see items 1603 and 1602) and output

image address section (see item 1606)) in respectively, processed image data corresponding to a portion of a processed image and a position of said processed image data within the processed image (see col. 17, lines 56-67 and see Fig. 30); and

a data flow control, coupled to said first and second processors, for coordinating the operation thereof (see Fig,. 30, the control circuit 1607 controls the arithmetic step which comprises multiple processors).

With regard to claim 13, Mita et al discloses an output image data memory (see fig. 30, item 1602); and

an output image address memory, the output image address memory for storing a position of the image data in the output image data memory relative to the image (see 18, lines 1-11).

Claim 14 is similarly analyzed and rejected the same as claim 2.

Allowable Subject Matter

3. Claims 4 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other Prior Art Cited

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. (4734782), (6145060), (6340973) and (6356314).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOSEF KASSA whose telephone number is (571) 272-7452. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JINGGE WU can be reached on (571) 272-7429. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communication and (571) 273-8300 for after Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service office whose telephone number is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PATENT EXAMINER

Yosef Kassa

12/6/05.

SAMIR AHMED
PRIMARY EXAMINER